IMPLEMENTATION OF CASCADED ARCHITECTURE FOR MEMRISTOR CROSSBAR ARRAY BASED NEUROMORPHIC COMPUTING

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ABSTRACT:

Neural networks, one of the main artificial intelligence technologies today, have the computational power and learning ability similar to the brain. However, implementation of neural networks based on the CMOS von Neumann computing systems suffers from the communication bottleneck restricted by the bus bandwidth and memory wall resulting from CMOS downscaling. With the advances of nanotechnology, the memristors based designs have been widely used in many applications such as mixed- signal design, non-volatile memories, CNN- Architectures. Multiply-accumulate calculations using a memristor crossbar array is an important method to realize neuromorphic computing. However, the memristor array fabrication technology is still immature, and it is difficult to fabricate large-scale arrays with high-yield, which restricts the development of memristor-based neuromorphic computing technology. Therefore, cascading small-scale arrays to achieve the neuromorphic computational ability that can be achieved by large-scale arrays, which is of great significance for promoting the application of memristor-based neuromorphic computing. To address this issue, we present a memristor-based cascaded framework with some basic computation units, several neural network processing units can be cascaded by this means to improve the processing capability of the dataset.

***Key words*: CNN, Crossbar array, Memristor, Cascaded Architecture**

I. INTRODUCTION

Many types of NNs have been used in the last three decades. Each type of NN is suitable for certain applications. Deep neural networks (DNN) are used for

applications such as autonomous cars for path recognition, learning systems, and skin cancer classifications. Recurrent neural networks are used for forecasting and classification. Moreover, critical-based neural networks utilize a supervisor to evaluate the performance of the network, based on as specific cost function. This type of network is used for robust optimal tracking control and data-driven control systems.

Convolutional neural networks (CNNs) have been broadly used in computer vision tasks such as image classification, they are widely popular in industry for their superior accuracy on datasets. Some concepts about CNNs were proposed by Fukushima and Miyake in 1980. In 1998, LeCun et al. proposed the LeNet-5 architecture based on a gradient-based learning algorithm. While moving ahead with deep learning algorithms, the complexity and dimension of network layers have grown markedly.

Therefore, cascading small-scale arrays to achieve the neuromorphic computational ability that can be achieved by large-scale arrays, which is of great significance for promoting the application of memristor based neuromorphic computing. In this paper, we present a memristor-based cascaded framework with some basic computation units, several neural network processing units can be cascaded by this means to improve the processing capability of the dataset. The basic computation unit builds on our prior work, which has validated this simplified three-layer CNNs can get desired recognition accuracy.

II. MEMRISTOR BASICS

Three fundamental passive elements such as resistor, capacitor, and inductor are currently used to build electronic circuits. The fourth fundamental element called memristor has recently emerged. The memristor was originally proposed in 1971, however remained largely a theoretical concept until the demonstration of actual fabricated devices exhibiting the characteristics of a memristor by HP labs in 2008. The new two-terminal passive element is named memristor as it combines the behavior of a memory and a resistor (i.e. memory + resistor). One of the basic properties, resistance, of a memristor depends on the magnitude, direction, and duration of the voltage applied across its terminals. Memristor remembers its most recent resistance value when applied voltage was turned off and until the next time.

when applied voltage is turn on. Memristor has several interesting properties including pinched hysteresis and dynamical-negative resistance that can have significant impact on nanoelectronics. All four fundamental elements along with the memristor are presented in Fig. 2.1 for a comparative perspective.

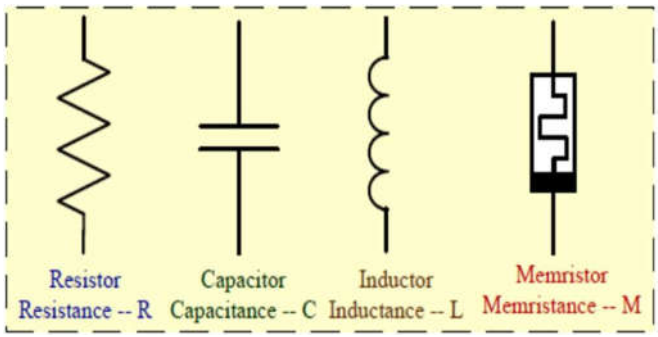

Fig 2.1 Memristor: The 4th Fundamental Element.

The fundamental-electrical elements need to be discussed in the context of the fundamental-electrical variables, voltage (v), current (i), charge (q), and flux (φ) for clear understanding. The relations of fundamental elements and variables are presented in Fig. 1.2. Memristor is characterized by its memristance (M). This

is described by the charge-dependent rate of change of flux with charge as follows: M(q) = (dΦm/dq). This property is similar to the fundamental element resistor which is characterized by its resistance (R). The other fundamental elements, inductor has inductance (L) and capacitor has capacitance (C) as their basic properties. It may be noted that the memristance is like a variable resistance. A battery can be considered to have memristance. However, the battery is an energy source and an active element, whereas the memristor is a passive element.

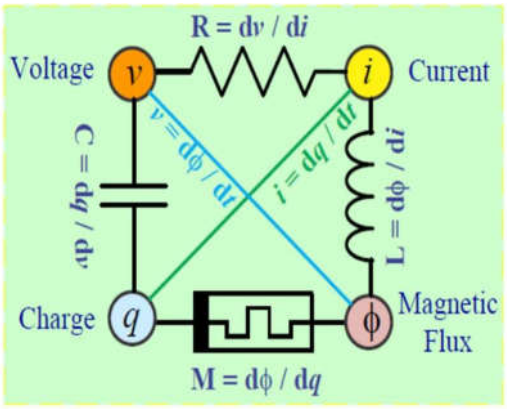

Figure 2.2: Memristor directly relates magnetic flux and charge; the missing connection among the 4 variables, v, i, q, and φ.

III. MEMRISTOR EMULATORS

A memristor emulator circuit which is designed with off-the-shelf solid-state components is presented. As the memristors are not commercially available so far, some circuit replacements which behave like memristors are needed to develop application circuits.

Some important features which should be included in any memristor emulator are 1) the memristance (resistance of memristor) should be programmable, 2) non-volatile, and 3) it can be connected to other circuit elements.

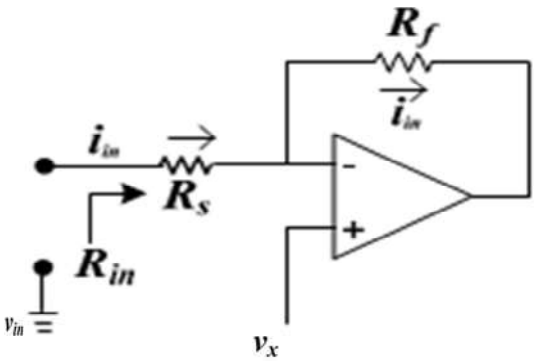

Fig. 3. Memristor emulator. Input resistance as a function of voltage v_x

Where i_{in} is the input current, R_s is a resistance at the inverting input terminal and v_x is the applied voltage at positive terminal of the op amp.

Assume that the voltage v_x is proportional to input current I_{in}, then

$$v_{in} = R_s i_{in} + m i_{in} = (R_s + m) i_{in}$$

Th implies that the input resistance of the circuit is Rs+m. If we can control m so that it is time integral of the input current i_{in}, then, the circuit in Fig. 3 acts as a memristor.

IV. IMPLEMENTATION

The standard ‘‘M-N-P’’ cascaded architecture is demonstrated in Fig. 4. The framework consists of several basic computation units (BCU) in series or in parallel. The memristor cascaded framework has been developed using memristor crossbar array technique by opamps. In the cascaded framework, the BCU is taken as an image transformation.

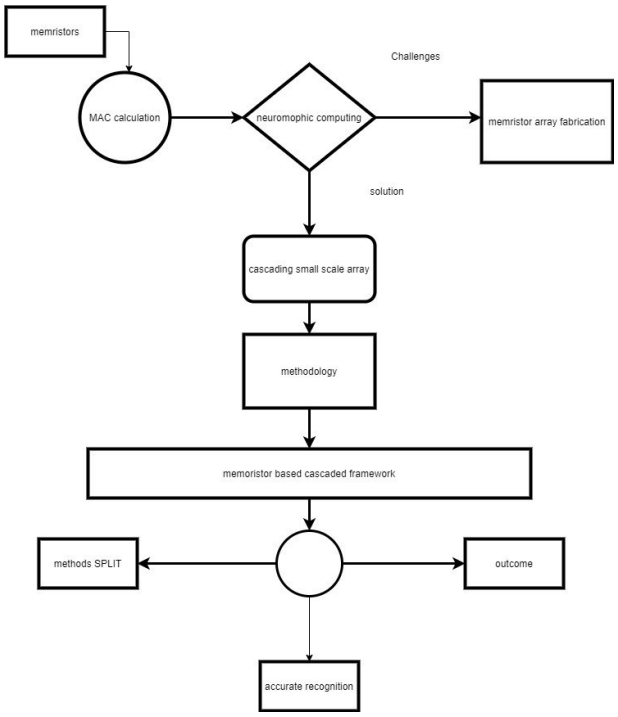

Fig 4.1 Block Diagram of Proposed System

In this paper we have implemented cascaded architecture which is based on memristor crossbar arrays for neuromorphic applications. The memristor crossbar array has been implemented using memristor emulators technique which can be achieved by Opamps.

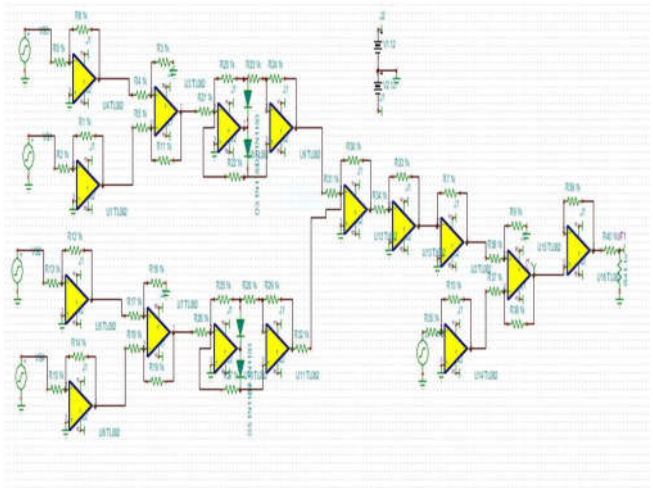

Fig 4.2 Cross bar array architecture

The Opamp based Memristor cross bar have been developed by using TINA TI software and has been simulated.

Also, Activation functions like tanh and rectilinear functions have been constructed and simulated in order determine the output of neural network like yes or no. These activation functions are used to determine the output of neural network like yes or no. It maps the resulting values in between 0 to 1 or -1 to 1 etc. (depending upon the function).

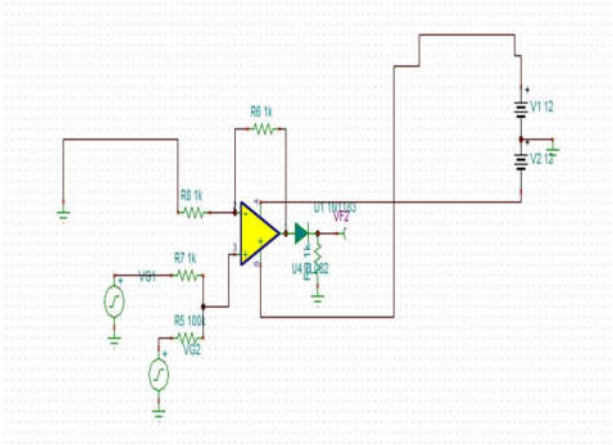

Fig 4.3 Relu Activation Function

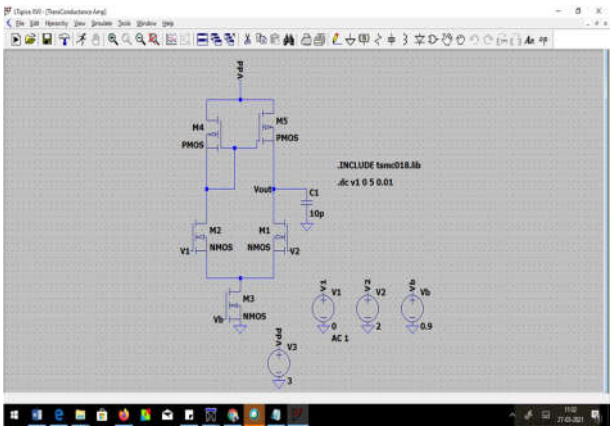

Fig 4.4 Circuit of Tanh Activation Function.

Memristor crossbar array structure has been developed and simulated using LTSPICE. Figure 4.5 represents the memristor crossbar array architecture.

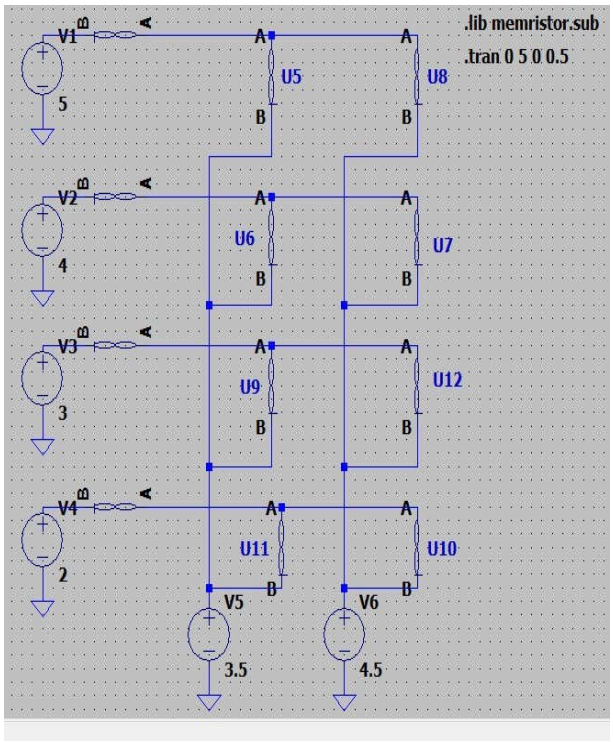

Fig 4.5 Memristor crossbar array

The standard cascaded architecture is demonstrated. The framework consists of several basic computation units (BCU) in series or in parallel. Memristor based cascaded framework has been developed using memristor emulators concept which can be achieved by op-amps. Input representing an image with specific voltages have been provided to the framework. Multiple accumulate calculations have been performed. Output representing increased accuracy is produced.

V. RESULTS

In this section results of cascaded framework, activation functions like tanh, relu units, memristor crossbar array have been described.

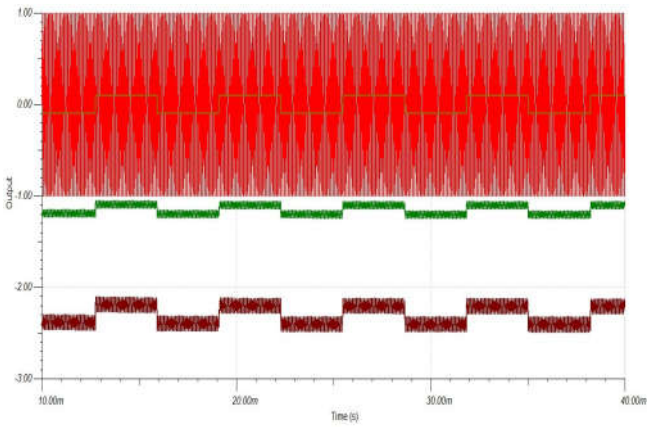

Fig 5.1 Output of opamp based cascaded framework.

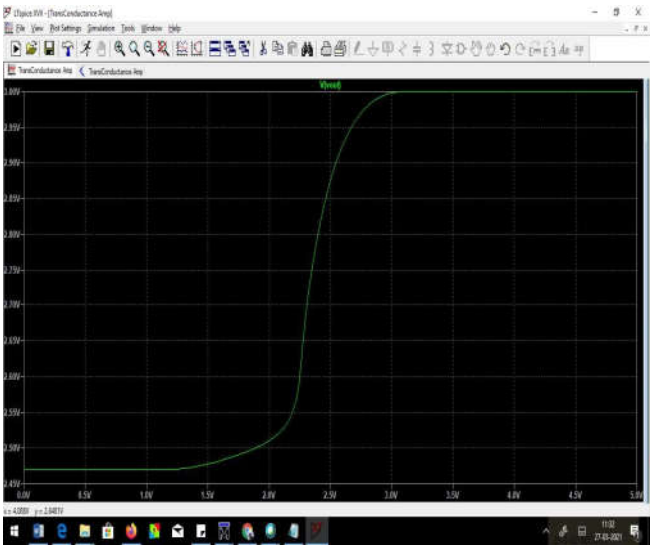

Fig 5.2 Output of Tanh function

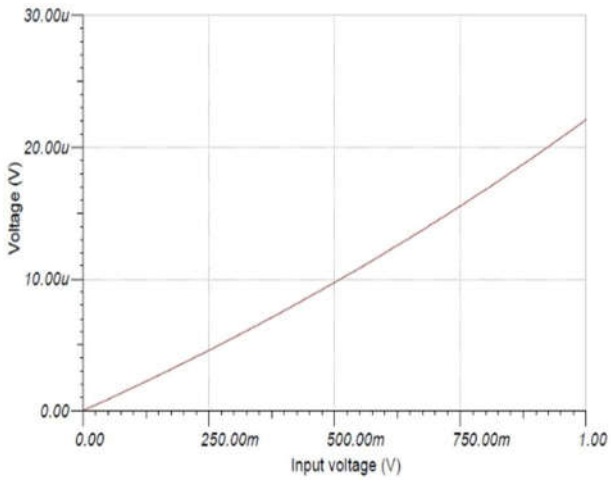

Fig 5.3 Transfer Characteristics of relu activation function

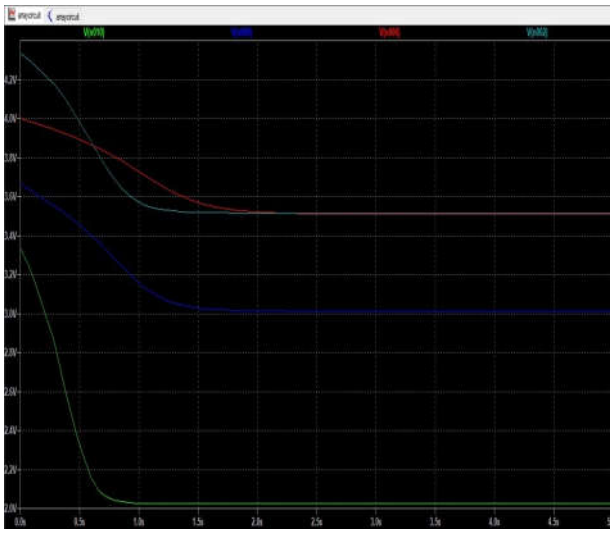

Fig 5.4 Output of Memristor crossbar array

VI. ANALYSIS

Advantages:

- Consumes less power since the switching activity is reduced.
- Increase the reliability.
- Reduce the critical.
- Low Complexity.

Applications:

- Cancer Diagnosis
- Industry Automation
- Image classification
- Shopping malls
- Prosthesis

VII. CONCLUSION

In this project, we propose a memristor-based cascaded framework, which can use several basic computation units in cascaded mode to improve the processing capability of the dataset. We demonstrate the architecture of the BCU and corresponding circuit structure. Based on the proposed BCU architecture, we present a‘‘M-N-P’’cascaded specially designed for improving recognition accuracy of the datasets, and we introduce a split method about BCU to reduce pressure of input terminal. Compared with VGGNet and GoogLeNet, the proposed cascaded framework can achieve desired accuracy with fewer parameters. Extensive circuits experiments are conducted show that the circuit simulation results can still provide a high recognition accuracy. For future work, we consider to further evaluate the cascaded framework on other tasks such as object detection.

VIII. FUTURE SCOPE

Neuromorphic computing finds a great deal of application in the medical diagnosis and classification section. Naturally this domain require a huge computation

power and resources. Modeling of neural network open a new horizon in the field of computational neuroscience. This require a very less power for computation and it provides more reliability and speed for computation.

This memristor based neuron modeling for computational array provides an efficient computational platform for higher efficiency. It finds its application in the robotics and in medical diagnosis.

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